Doc Code: AP PRE REQ

PTO/SB/33 (07-05)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
0107262.00199US1 7090/P0	

Application Number	Filed
10/623665-Conf. #5061	July 21, 2003
First Named Inventor: Lawrence C. WEST et al.	
Art Unit: 2813	Examiner: J. M. Dolan

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant /inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [ ] attorney or agent of record. Registration number _____
- [x] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. 32,590

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July 21, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of 1 forms are submitted.

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: MS AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: July 21, 2006 Signature: Maureen DiVito (Maureen Divito)

The Examiner rejected claims 32, 34, 35, 48-53 under 35 U.S.C. §103(a) as being unpatentable over U.S. 5,987,196 (Noble) in view of U.S. Patent Application 2002/0146865 A1 (Hoel) and U.S. 5,098,861 (Blackstone).

The Examiner admits that "Noble does not disclose sending the optical-ready substrate to a purchaser that will subsequently fabricate the microelectronic circuitry thereon, but rather, uses the same entity for fabricating both the optical signal circuitry and the microelectronic circuitry." To supply that which is missing from Noble, the Examiner relies on the other two references about which he has the following to say:

> Hoel teaches that it is beneficial to partially fabricate portions of integrated circuits shared among many final integrated circuit designs, store the partially fabricated circuits in inventory, and later customize the circuits using a second set of fabrication processes, in order to improve cost and processing time...
>
> Blackstone teaches that it is known to partially fabricate a semiconductor wafer and then sell the partially fabricated wafer to a semiconductor manufacturer, who then will complete the fabrication process...
>
> It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the method of Noble, such that a second entity performs the microelectronic circuitry fabrication after purchasing the partially finished substrate, as suggested by Hoel and Blackstone...

The Hoel Patent

With regard to Hoel, we note that contrary to what the Examiner seems to believe it has no applicability to Noble, at least not in the manner proposed by the Examiner. Hoel involves semiconductor circuits that are customizable, i.e., integrated circuits in which the underlying, already fabricated microelectronic devices can be interconnected in different ways depending on the customized mask that is used.

The customization to which Hoel refers involves forming only those vias and metalizations that are necessary to interconnect desired already-fabricated microelectronic devices and refraining from forming other vias that are possible but not appropriate for the particular customized design that is being fabricated. In other words, Hoel teaches customizing the metal interconnect phase of the fabrication process, which occurs after all of the underlying microelectronic devices have been fabricated. Hoel's technique assumes that the underlying arrangement of microelectronic devices is the same for the different possible customized circuit

designs. The only thing that changes is the way in which those underlying circuit devices are interconnected.

Thus, if a person skilled in the art one were to combine the teachings of Hoel with Noble, that person would end up with a process that was completed up to the point just before the vias and metalization interconnects are to be formed. Stated differently, one would modify Noble's fabrication process in a way that only affects how the microelectronic devices that are fabricated in the upper layer are interconnected. But that is not what is claimed. In other words, the result of that combination would **not** be a process in which the optical circuitry is fabricated and then the resulting substrates are put into inventory for use at a later time to fabricate the overlying electrical circuitry, as the Examiner has argued.

Hoel does not teach nor does he in any way suggest splitting the fabrication process into two phases, during the first of which one set of circuit components (e.g. optical components) is fabricated and during the second of which a second set of circuit components (e.g. microelectronic components) is fabricated. Indeed, Hoel does not in any way suggest applying his technique to any phases of the fabrication process other that the phase during which vias and metal interconnects are fabricated. In addition, neither Hoel nor any of the other references relied on by the Examiner, teaches or suggests that underlying optical circuitry that is fabricated in Noble could be standardized arrangements that would support different customized arrangements of microelectronic circuitry that are to be fabricated in layer 20 of the Noble structure.

It is inappropriate for the Examiner to simply conclude, without any clear suggestion in the prior art for doing so, that it is obvious to move that dividing line between the two phases of Hoel's fabrication process to a point at which the fabrication of the optical circuitry has been completed and the fabrication of the microelectronic circuitry is about to begin. That there might be advantages to doing so does not *per se* render that combination obvious. There must be some basis for concluding that the advantages arising out of that particular approach were appreciated before the time of the present invention.

In short, there is no motivation to combine Hoel with Noble in the manner proposed by the Examiner. But if a person of ordinary skill in the art were to combine Hoel with Noble, the result would not be the claimed invention.

The Blackstone Patent

With regard to Blackstone, we note that the "partially fabricated wafers" that Blackstone proposes be sold have no circuits in them. Indeed, they do not even have any devices in them. They are simply substrates in which two buried layers have been formed beneath an upper layer of silicon, namely, a silicide layer on top of a SiO_2 or SiN layer. The silicide layer provides a fast diffusion path for later diffusion of N+ or P+ dopants into the wafers to form high conductivity buried layers that have uniform thickness. Backstone teaches nothing more that providing substrates that have been modified to accommodate the later fabrication of complimentary semiconductor structures. According to Blackstone:

> The metal silicide layer disposed internally to the bonded semiconductor substrate enables conventional semiconductor planar fabrication technology to form a buried layer in the first semiconductor wafer which is shallow, and of uniform thickness. (Col. 3, lines 13-17).

Blackstone's process is very similar to what is done in fabricating an SOI wafer in which the upper silicon layer is provided for later fabricating microelectronic circuitry and a buried thin layer of insulating material, e.g. SiO_2, is provided to isolate the upper silicon layer from the rest of the silicon substrate. Clearly, the idea behind Blackstone is to provide the semiconductor fabricator with a substrate that does not constrain the fabricator with regard to the layout of the circuits that can be fabricated into the substrates.

Blackstone neither teaches nor suggests fabricating some circuitry in a buried layer before providing the substrate to another entity, which then fabricates further circuitry in an overlying layer. Indeed, Blackstone teaches away from customizing the preliminary fabrication process in any way that results in a substrate that is not "generic." Blackstone makes this clear in his discussion of the drawbacks of the prior art approaches:

> One drawback of this technique is that wafer 70, FIG. 3A, becomes "customized" immediately upon the first doping and diffusion steps 72-74 shown in FIG. 3A. Accordingly, the prior art lacks a method for processing one or more semiconductor wafers to provide a semiconductor substrate that is "generic" or partially processed utilizing more sophisticated semiconductor processing techniques, while allowing the partially processed substrate to be subsequently further processed and finished utilizing conventional semiconductor planar processing techniques, thus insuring that the substrate will provide matched semiconductor elements or devices of equal thickness. (Col. 2, lines 50-62).

Thus, a person of ordinary skill in the art would not be motivated to employ the techniques of Blackstone in the manner proposed by the Examiner. The Examiner's proposed

modification of Nobel's fabrication process would yield partially completed structures that could not even remotely be characterized as generic, which is a result that is contrary to the teachings of Blackstone.

However, even if one were motivated to employ Blackstone's techniques in the fabrication of Noble's structures, the result would be a substrate that has been modified in some way that is useful to subsequent processing of the circuitry (both optical and electrical) that is to be later fabricated into that substrate. That is not the claimed invention.

Conclusions

None of the references on which the Examiner has relied even hints at developing an "optical ready substrate" i.e., a substrate into which the optical circuitry has been fabricated for another entity which will subsequently add the overlaying microelectronic circuitry which uses that optical circuitry.

The Examiner has cited no prior art that suggests providing optical signal circuitry above which "customizable" microelectronic circuitry would or could be fabricated. Without any teaching or suggestion of that concept, there is no motivation to apply Hoel so as to split the fabrication process at a point before which the optical signal circuitry has been fabricated and after which microelectronic circuitry is yet to be fabricated and provide the unfinished substrate to another entity to complete the fabrication process.

We remind the reader that one of the two references on which the Examiner relies involves preparing a substrate before any microelectronic or optical circuitry whatsoever is fabricated into it (i.e., the front end of the process) while the other reference involves performing all of the processing up to the point at which the fabricated devices are to be interconnected (i.e., the backend of the process). But the Examiner has cited no reference that in any way suggests halting the fabrication at some stage in the middle (i.e., after some devices have been fabricated but before other devices have been fabricated) and the providing the unfinished substrate to another entity to complete the fabrication process. So, the Examiner has no legitimate basis for concluding that it would be obvious to prepare an optical ready substrate and then provide that substrate to a purchaser which will then fabricate the microelectronic devices.

It might be true that the advantages of such a substrate are readily apparent after the fact. It might also be true that fabricators in the past have made microelectronic circuits in which the metallization was not provided so that a purchaser could connected the underlying microelectronic components in whatever way they wanted (as suggested by Hoel). But the Examiner has provided no prior art which supports the proposition that anybody has, until the present invention, thought about, considered, or suggested applying those concepts in the way that is presently claimed.

The present invention addresses a serious obstacle to integrating optical circuitry and microelectronic circuitry into the same chip. That obstacle, which was first truly appreciated by the present inventors, is the reluctance of microelectronic circuitry fabricators to tinker with their processes to accommodate techniques required to fabricate the optical circuitry. The present invention provides a solution to overcoming that obstacle. The microelectronic circuitry fabricators, such as Intel or TSMC, need not significantly modify their processes with the present invention. The optical circuitry is fabricated in the wafer and then an upper layer is added "that is of a sufficient quality to permit microelectronic circuitry to be fabricated thereon."

For the reasons presented above, we submit that the claims are allowable and request that application be permitted to issue.